DS15BR400EVK

Quad LVDS Buffer/Repeater with Pre-emphasis

Evaluation Kit User Manual

August 2006
Rev 0.3

Overview

DS15BR400 is a four channel LVDS Buffer/Repeater, featuring pre-emphasis with maximum pre-emphasis gain of approximately 6 dB at 750 MHz. The device has internal 100-ohm resistors on both, the inputs and outputs, to improve performance and minimize board size. It utilizes LVDS technology for low power, high-speed and superior noise immunity.

The purpose of this document is to familiarize you with the DS15BR400 Evaluation Board (DS15BR400EVK), suggest the test setup procedures and instrumentation, and to guide you through some typical measurements that will demonstrate the performance of the device.

Description

Figure 1 below represents the top layer drawing of the board with the silkscreen annotations. It is a four by four inch six layer printed circuit board (PCB) that has a single-device layout capable of demonstrating performance and all functions of the DS15BR400.

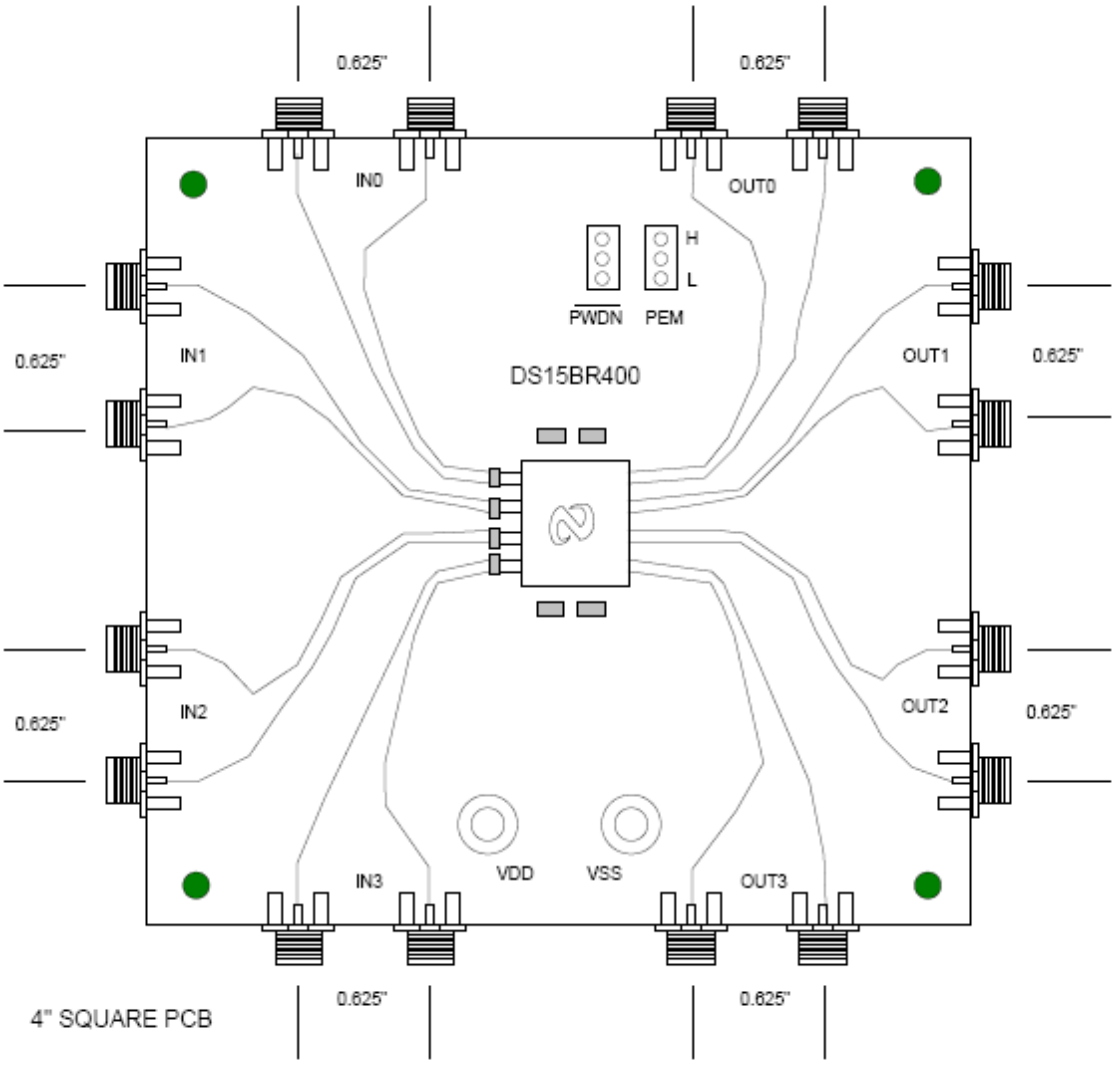


Figure 1: DS15BR400 Evaluation Board - Top View

All LVDS inputs and outputs are accessible through SMA connectors and suitable for connections to 50-ohm instrumentation. The power can be applied using banana plugs. The control pins, PWDN* and PEM pins, are connected to 2-position switches.

Test Setup Procedure

The following is a recommended test setup procedure for the device evaluation. Figure 2 depicts a typical setup and instrumentation used for the device evaluation.

1. Apply the power to the device (3.3V typical) between VDD and VSS banana plug receptacles, observe the value of $I_{CC,}$ and compare it with the expected value (refer to the datasheet) to ensure that the device is functional.

2. Select I/O pairs you want to evaluate. For example, let's say that we want to evaluate the IN0 to OUT0 signal path of the DS15BR400. The setup instructions that follow are based on this selection.

3. Connect a signal source (i.e. signal generator or an LVDS driver) to the IN0 inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations.

4. Enable the DS15BR400 by setting PWDN* to high on CON1. Optionally, you may turn the pre-emphasis on for this output by setting PEM to "H" position on CON2.

5. Connect the OUT0 outputs to an oscilloscope and view the output signals with an oscilloscope with the bandwidth of at least 3 GHz.

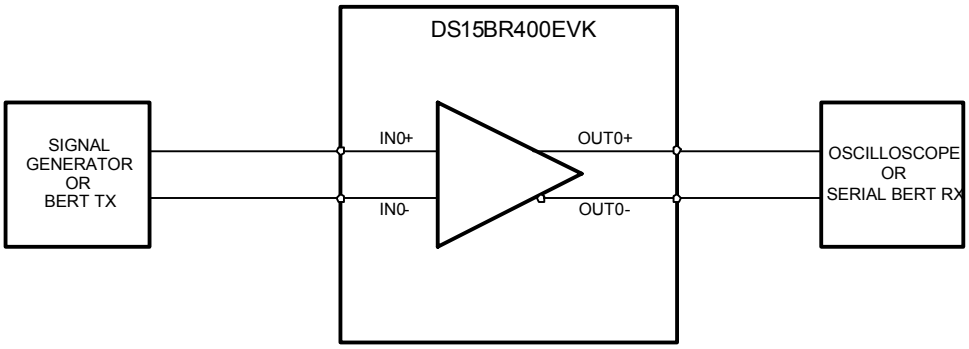


Figure 2. Typical Test Setup

Figure 3 and 4 show an output eye diagram obtained using the DS15BR400EVK setup as in figure 2. The input was 400mV in amplitude with 1.2 V common mode voltage 1.5 Gbps NRZ PRBS-23.

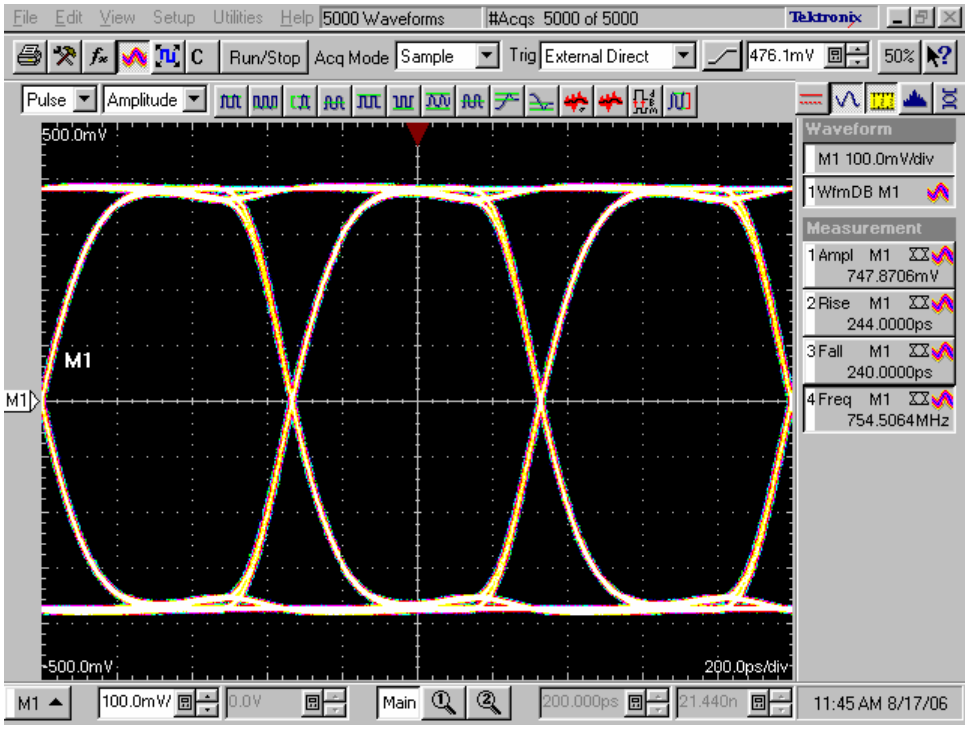


Figure 3. DS15BR400– Output Eye Diagram, Pre-emphasis OFF

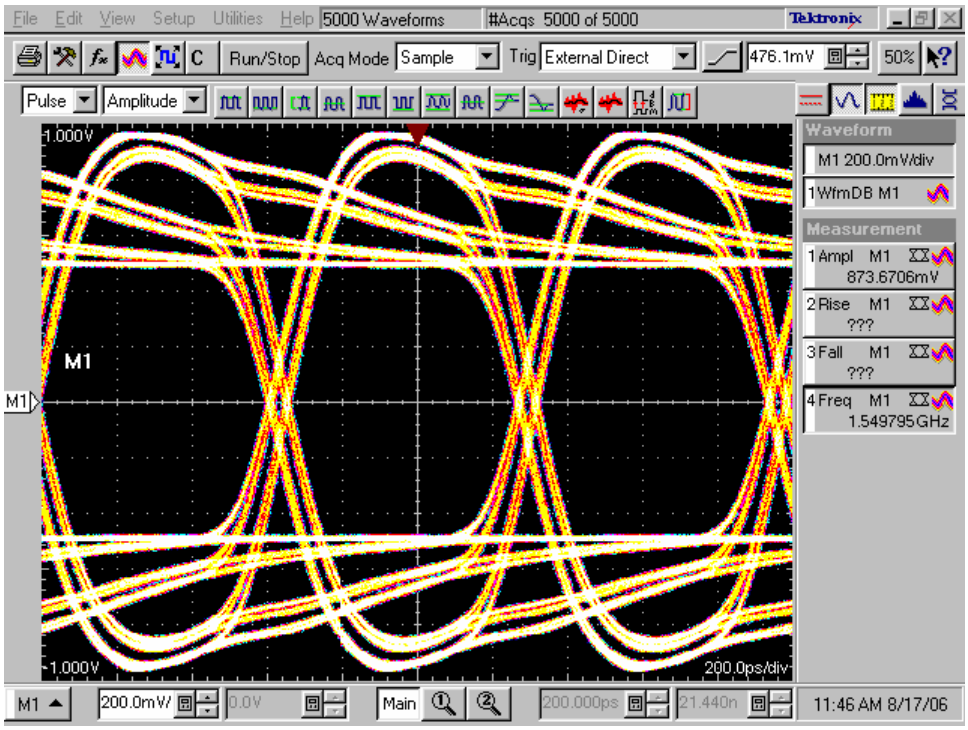


Figure 4. DS15BR400 – Output Eye Diagram, Pre-emphasis On

Figures 5 and 6 show the eye diagrams obtained at 2 Gbps with NRZ PRBS-23.

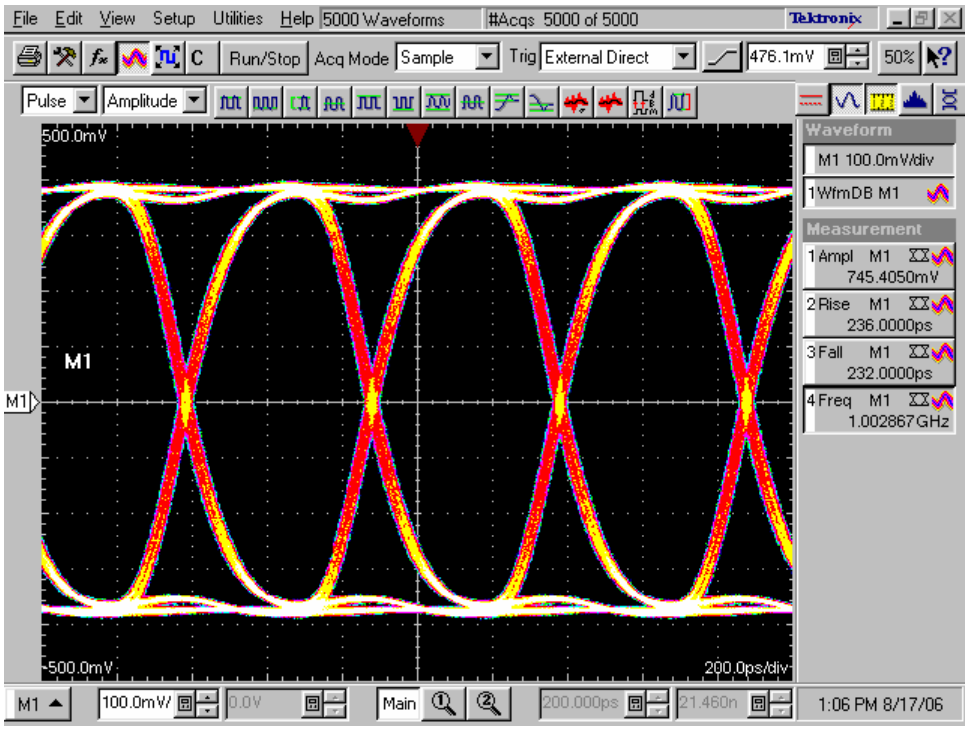


Figure 5. DS15BR400– Output Eye Diagram, Pre-emphasis OFF

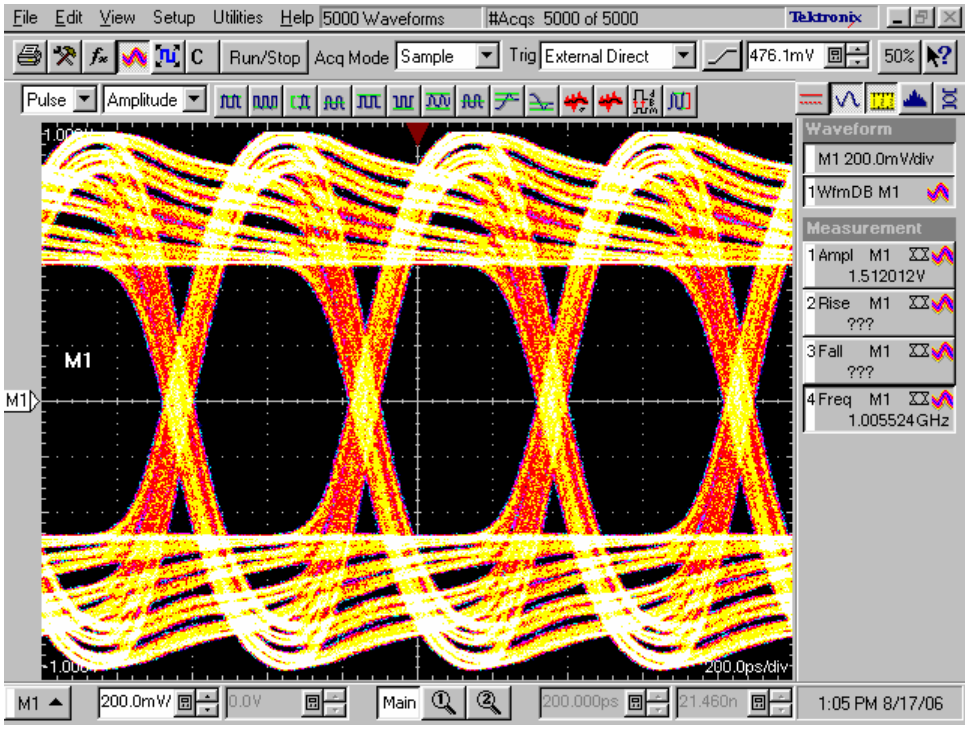
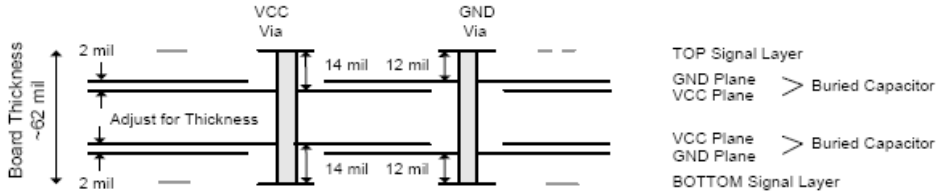


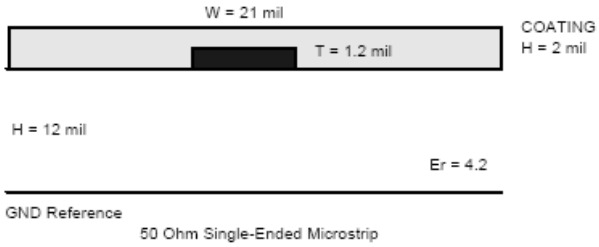
Figure 6. DS15BR400 – Output Eye Diagram, Pre-emphasis On

Bill Of Materials

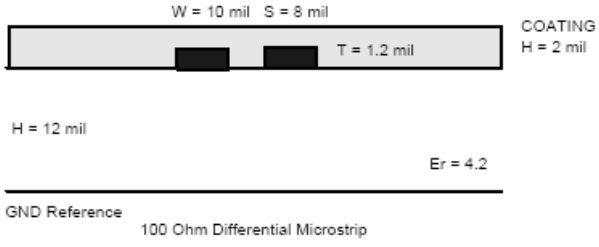
DS15BR400 APPLICATION EVALUATION BOARD							
Revised: May 21, 2006							
Item	**Part Type**	**Part Number**	**Mfg**	**Description**	**Qty**	**Ref Des**	**Notes**
1	CONN		ANY	HEADER3X1	2	CON1,CON2	
2	CONN	50F1460	NEWARK	JACK, Banana Plug Receptacle	2	CON3,CON4	
3	CAP		ANY	0.01□F,±10%, 0603	2	C1,C4	
4	CAP		ANY	□□F, ±10%,0603	1	C2	
5	CAP		ANY	0.1µF, ±10%, 0603	1	C3	
6	CAP		ANY	22µF, ±10%, 7343	1	C5	
7	RES		ANY	100 Ohm	4	R1-R4	
8	CONN	99F6798	NEWARK	SMA, 50 Ohm, End Launch	16	SMA1-SMA16	
9	IC		NAT	2 GHz 4 Channel Buffer/Repeater	1	U1	

PCB Stack Up



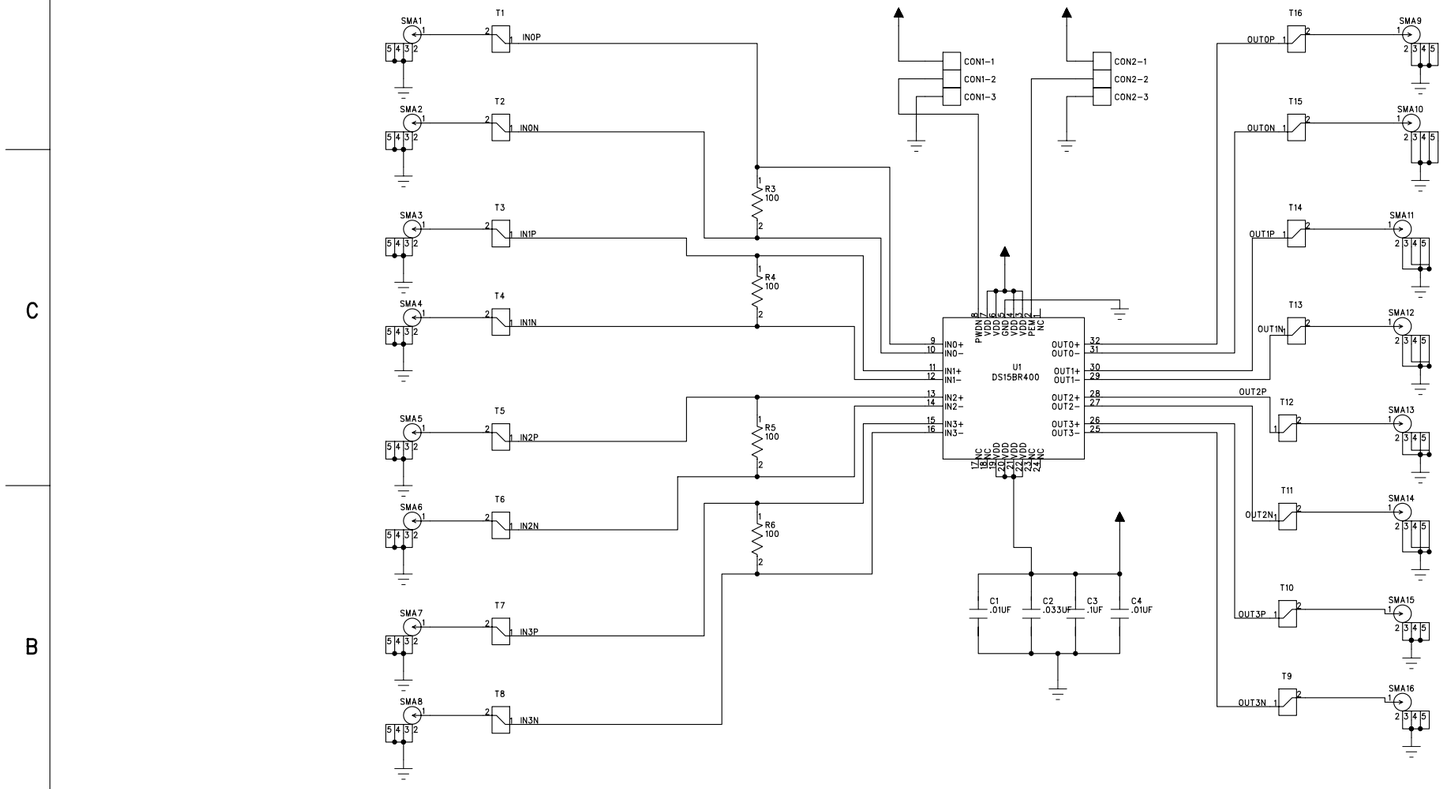


50 Ohm Single-Ended Microstrip

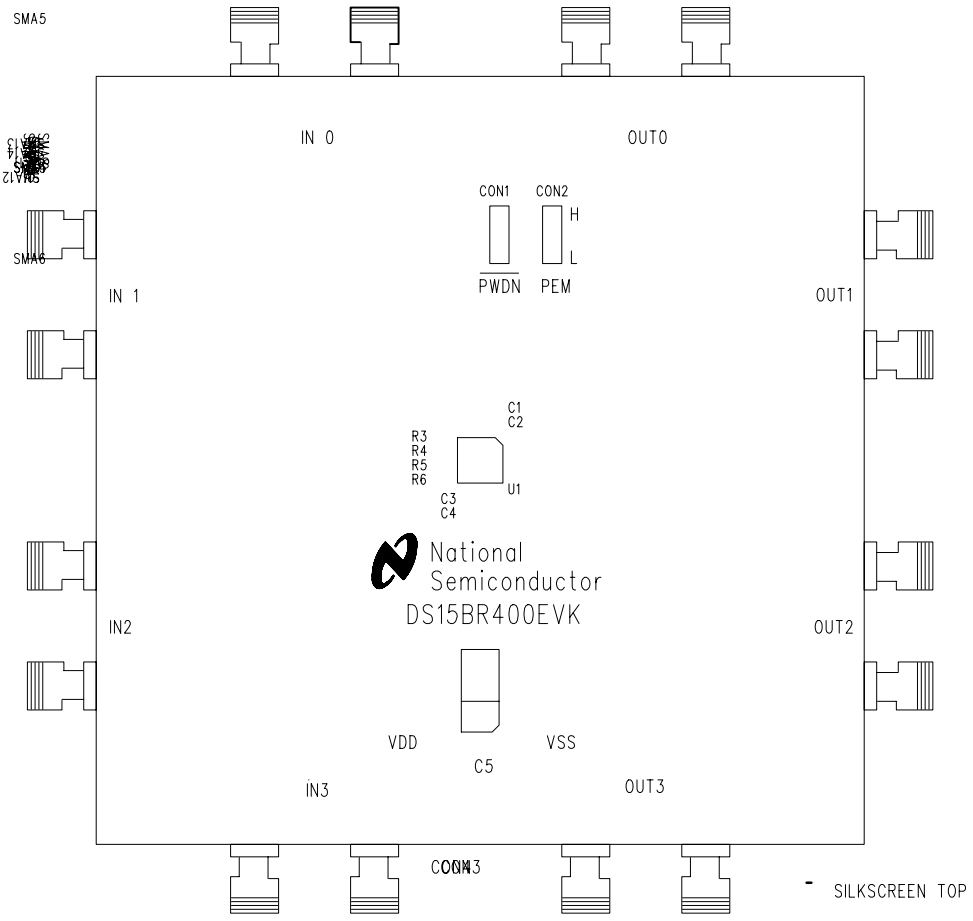


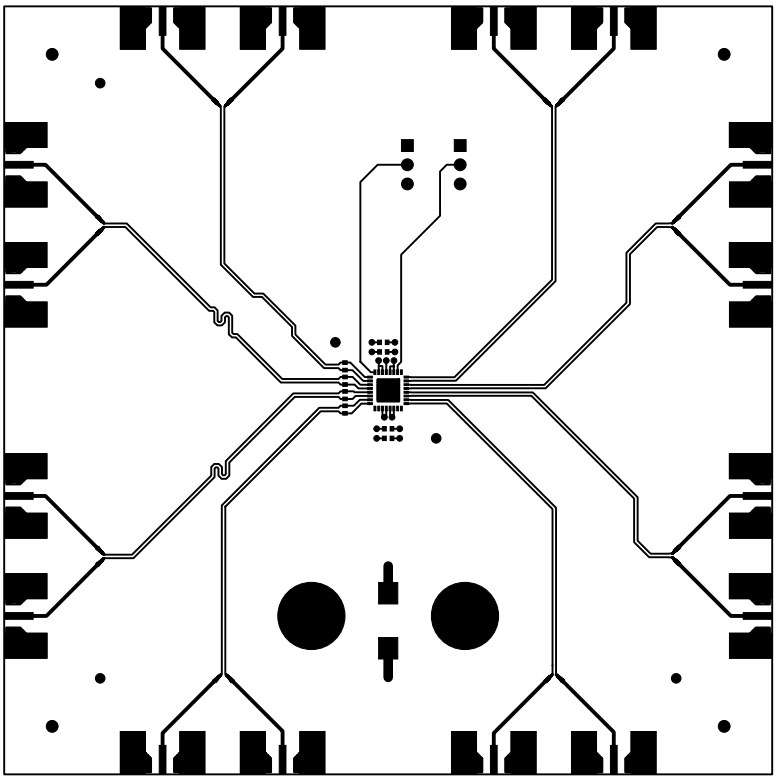
100 Ohm Differential Microstrip

REVISION RECORD			
LTR:	ECO NO:	APPROVED:	DATE:

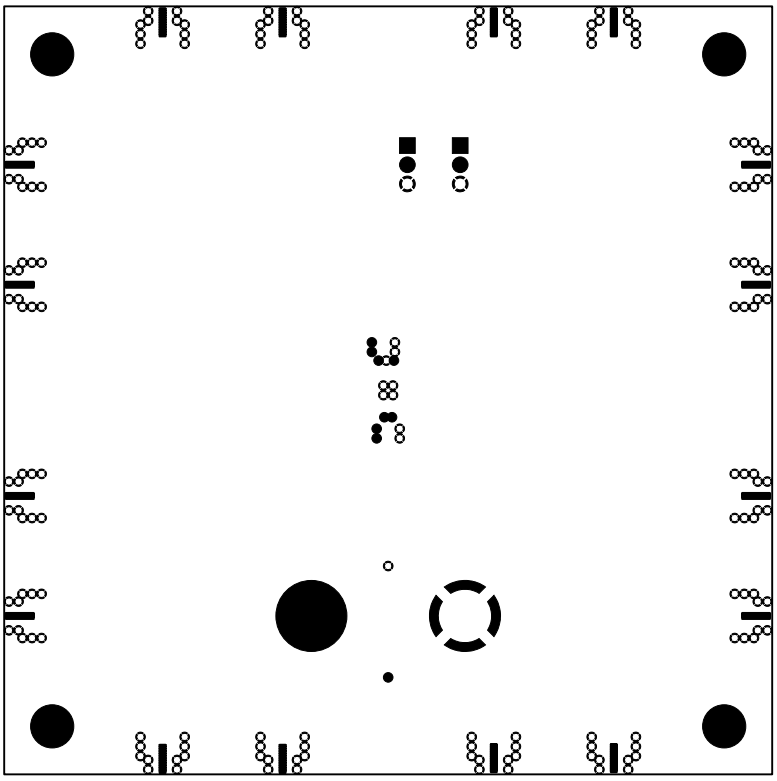


Enercon Technologies — 25 NorthBrook Drive, Gray, Maine 04039 U.S.A.		COMPANY: NATIONAL SEMICONDUCTOR	
DRAWN: ACF	DATED: 6/14/06	TITLE: SCHEMATIC 15BR400EVK EVALUATION BD	
CHECKED:	DATED:	CODE:	SIZE: C / DRAWING NO: S-05136 / REV: 0
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: 1 OF 1

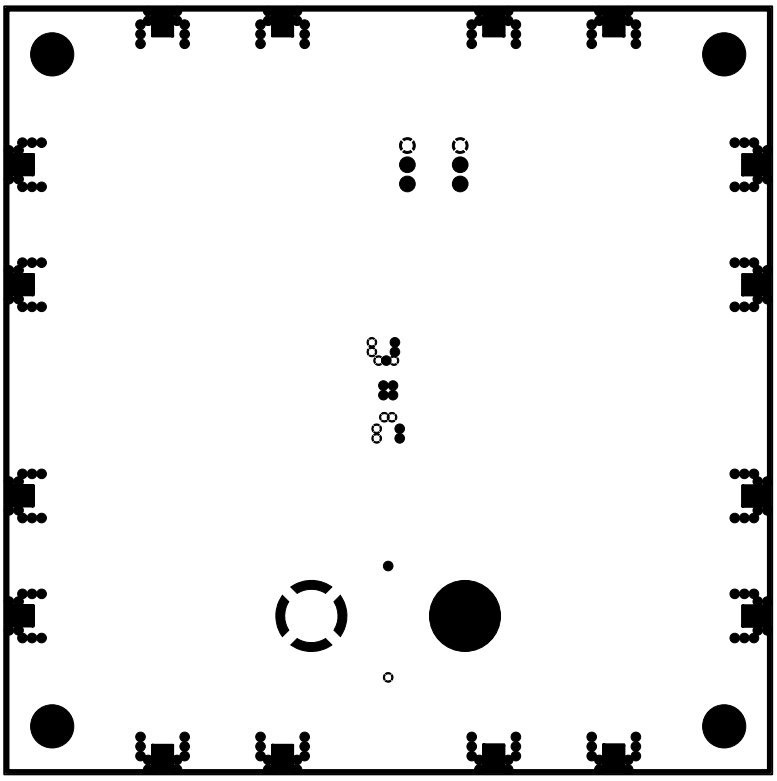

SMA5
IN 0
OUT0
CON1
CON2
H
L
SMA6
PWDN
PEM
IN 1
OUT1
C1
C2
R3
R4
R5
R6
U1
C3
C4
National
Semiconductor
DS15BR400EVK
IN2
OUT2
VDD
VSS
C5
IN3
OUT3
SILKSCREEN TOP



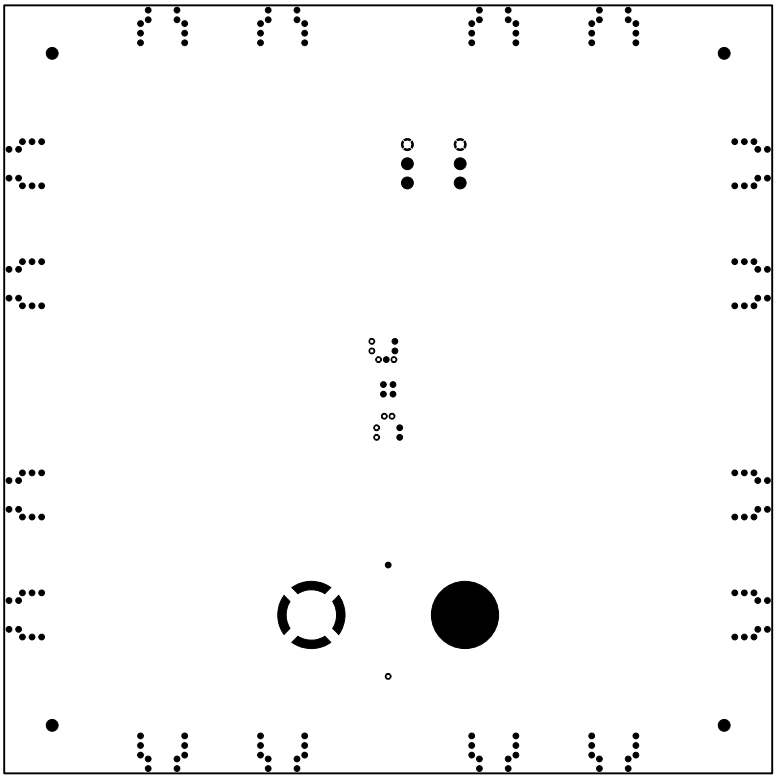
- LAYER 1- TOP



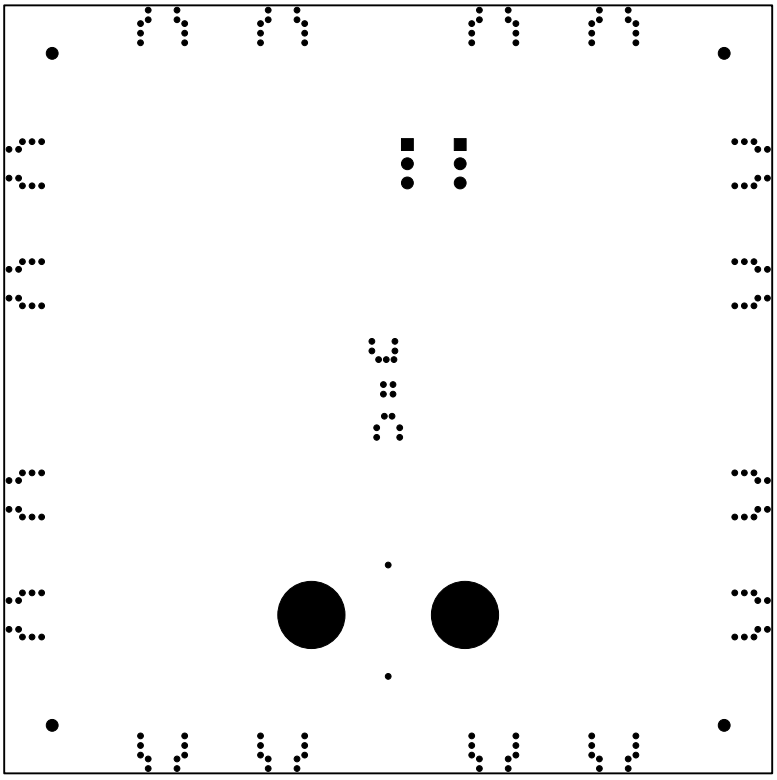
- LAYER 2 GND PLANE



- LAYER 3 VCC PLANE



- LAYER 4 VCC PLANE



- LAYER 5 GND PLANE

LAYER 4 - BOTTOM